IN THE CLAIMS

Listing of Claims:

1. (original) A method for providing a bi-directional communication bus between a first processing unit (PU) and a second and third PU each adjacent to the first PU and within M processing units (PUs), wherein the first PU is physically coupled to the second PU with a first Link input and a first Link output and to the third PU with a second Link input and a second Link output, the method comprising the steps of:

sending a first output signal from an output of the first PU to the third PU on the second Link output or selectively sending a second output signal received on the first Link input from the second PU to the third PU on the second Link output in response to the first logic state of a first enable signal;

selectively sending a third output signal received on the second Link input from the third PU or the first output signal from the first PU to the second PU on the first Link output in response to the first logic state of a second enable signal; and

receiving, in an input of the first PU, the third output signal received on the second Link input from the third PU or selectively receiving the second output signal on the first Link input from the second PU when the first enable signal has the first logic state.

2. (original) The method of claim 1, wherein the first and second enable signals are generated by control logic in the first PU.

3. (original) The method of claim 1, wherein communication between the second PU and the first and third PU is blocked when the first and second enable signals concurrently are at a second logic state.

4. (original) The method of claim 1, wherein the second PU has a second Link output coupled to the first Link input of the first PU and a second Link input coupled to the first Link output of the first PU.

5. (original) The method of claim 1, wherein the third PU has a first Link input coupled to the second Link output of the first PU and a first Link output coupled to the second Link input of the first PU.

6. (original) A bi-directional communication bus in each of M processing units (PUs) for bi-directional communication between a first processing unit (PU) and a second and third PU each adjacent to the first PU and within the M PUs, wherein the first PU is physically coupled to the second PU with a first Link input and a first Link output and to the third PU with a second Link input and a second Link output comprising:

circuitry for coupling a first output signal from an output of the first PU to the third PU on the second Link output or selectively coupling a second output signal received on the first Link input from the second PU to the third PU on the second Link output in response to the first logic state of a first enable signal;

circuitry for selectively coupling a third output signal received on the second Link input from the third PU or the first output signal from the first PU to the second PU on the first Link output in response to the first logic state of a second enable signal; and

circuitry for coupling the third output signal received on the second Link to an input of the first PU or selectively coupling the second output signal on the first Link input from the second PU when the first enable signal has the first logic state.

7. (original) The bi-directional bus of claim 6, wherein the first Link input and a first function output from function logic circuitry are coupled to communication logic circuitry generating a first function output signal on the first Link output and a first communication output signal on a first communication output.

8. (original) The bi-directional bus of claim 7, wherein the second Link input and the first communication output are coupled to the function logic circuitry generating a second function output signal on the first Link output and a second function output signal on a first function output.

9. (original) The bi-directional bus of claim 8, wherein the first communication output signal is generated as a logic combination of the second output signal from the second PU and the first enable signal in a first logic gate.

10. (original) The bi-directional bus of claim 9, wherein the first function output signal is generated as a logic combination of the second function signal and the second enable signal in a second logic gate.

11. (original) The bi-directional bus of claim 10, wherein the second function signal is generated as a logic combination of the first communication signal and the first output signal in a third logic gate.

12. (original) The bi-directional bus of claim 11, wherein the second function signal is generated as the logic combination of the second function signal and the third output signal in a fourth logic gate.

13. (original) The bi-directional bus of claim 7, wherein the input of the first PU is coupled to the first function output of the function logic circuit.

14. (original) The bi-directional bus of claim 12, wherein the first and second logic gates are AND logic gates.

15. (original) The bi-directional bus of claim 12, wherein the third and fourth logic gates are OR logic gates.

16. (original) The bi-directional bus of claim 6, wherein bi-directional communication between the first and second PU are enabled by setting both the first and second enable signals to a logic one.

17. (original) The bi-directional bus of claim 6, wherein the first and second PUs are pattern detection processing units, each for comparing an input data byte to a pattern byte selected for a sequence of pattern bytes stored in each of the first and second PUs and generating a compare output in each of the first and second PUs, wherein the pattern byte in each of the PUs is selected by an address pointer and modified in response to a logic state of the compare output and an operation code stored with the selected pattern byte.

18. (original) The bi-directional bus of claim 17, wherein the bi-directional communication between the first PU and the second PU is enabled to allow increment signals from the first and second PU, for incrementing their respective address pointers, to be coupled to and logic combined in the control logic of the first PU and control logic of the second PUs to generate a modified increment address pointer signal at the PU input of the first PU and the one or more adjacent PUs.

19. (original) The bi-directional bus of claim 18, wherein the modified increment address pointer signal is used to enable advanced matching capabilities to be performed by the first and second PU by incrementing the address pointer in the first PU or the second PU if either the first or second PU generates a logic state on its corresponding compare output indicating that a particular input data byte has compared to either selected pattern byte in the first or second PU.

20. (original) A data processing system comprising:

a central processing unit (CPU);

a random access memory (RAM);

one or more parallel pattern detection engines (PPDEs);

a bus coupling the CPU, RAM, and the one or more PPDEs, wherein each of the PPDEs has an input/output (I/O) interface for coupling data into and out of the PPDEs, M pattern detection processing units (PUs), and a cascade system for providing a bi-directional communication bus circuitry in each of M PUs for bi-directional communication between a first processing unit (PU) and a second and third PU each adjacent to the first PU and within the M PUs, wherein the first PU is physically coupled to the second PU with a first Link input and a first Link output and to the third PU with a second Link input and a second Link output comprising:

circuitry for coupling a first output signal from an output of the first PU to the third PU on the second Link output or selectively coupling a second output signal received on the first Link input from the second PU to the third PU on the second Link output in response to the first logic state of a first enable signal;

circuitry for selectively coupling a third output signal received on the second Link input from the third PU or the first output signal from the first PU to the second PU on the first Link output in response to the first logic state of a second enable signal; and

circuitry for coupling the third output signal received on the second Link to an input of the first PU or selectively coupling the second output signal on the first Link input from the second PU when the first enable signal has the first logic state.

21. (original) The data processing system of claim 20, wherein the first Link input and a first function output from function logic circuitry are coupled to communication logic

circuitry generating a first function output signal on the first Link output and a first communication output signal on a first communication output.

22. (original) The data processing system of claim 21, wherein the second Link input and the first communication output are coupled the function logic circuitry generating a second function output signal on the first Link output and a second function output signal on a first function output.

23. (original) The data processing system of claim 22, wherein the first communication output signal is generated as a logic combination of the second output signal from the second PU and the first enable signal in a first logic gate.

24. (original) The data processing system of claim 23, wherein the first function output signal is generated as a logic combination of the second function signal the and the second enable signal in a second logic gate.

25. (original) The data processing system of claim 24, wherein the second function signal is generated as a logic combination of the first communication signal and the first output signal in a third logic gate.

26. (original) The data processing system of claim 25, wherein the second function signal is generated as the logic combination of the second function signal and the third output signal in a fourth logic gate.

27. (original) The data processing system of claim 21, wherein the input of the first PU is coupled to the first function output of the function logic circuit.

28. (original) The data processing system of claim 26, wherein the first and second logic gates are AND logic gates.

29. (original) The data processing system of claim 26, wherein the third and fourth logic gates are OR logic gates.

30. (original) The data processing system of claim 20, wherein bi-directional communication between the first and second PU are enabled by setting both the first and second enable signals to a logic one.

31. (original) The data processing system of claim 20, wherein the first and second PUs are pattern detection processing units, each for comparing an input data byte to a pattern byte selected for a sequence of pattern bytes stored in each of the first and second PUs and generating a compare output in each of the first and second PUs, wherein the pattern byte in each of the PUs is selected by an address pointer and modified in response to a logic state of the compare output and an operation code stored with the selected pattern byte.

32. (original) The data processing system of claim 31, wherein the bi-directional communication between the first PU and the second PU is enabled to allow increment signals from the first and second PU, for incrementing their respective address pointers, to be coupled to and logic combined in the control logic of the first PU and control logic of the second PUs to generate a modified increment address pointer signal at the PU input of the first PU and the one or more adjacent PUs.

33. (original) The data processing system of claim 32, wherein the modified increment address pointer signal is used to enable advanced matching capabilities to be performed by the first and second PU by incrementing the address pointer in the first PU or the second PU if either the first or second PU generates a logic state on its corresponding

compare output indicating that a particular input data byte has compared to either selected pattern byte in the first or second PU.

34. (original) A processing unit (PU) bi-directional communication bus coupling a processing unit PU(N) and a first adjacent PU(N-1) and second adjacent PU(N+1) within a group of M PUs, wherein each PU(N) has a bus circuit (BC) and a BC(N) in PU(N) is physically coupled to a BC(N-1) in PU(N-1) with a first Link input and a first Link output and BC(N) is coupled to a BC(N+1) in PU(N+1) with a second Link input and a second Link output, wherein BC(N) comprises:

function logic receiving a PU output signal PUO(N) from P(N), a first gated communication signal (GCS1) from PU(N-1), and a first communication signal (CS1) from PU(N+1) on the second Link input and generating a second communication signal (CS2) on the second Link output and a second gated communication signal (GCS2), wherein CS2 is a logic combination of the PUO(N) and GCS1 and GCS2 is a first logic combination of the CS1 and CS2; and

communication logic receiving a third communication signal (GS3) from the PU(N-1) and GCS2 and generating a fourth communication signal (GS4) on the first Link output and generating GCS1, wherein CS4 is a second logic combination of GCS2 and a logic state of a chain out signal and GCS1 is a logic combination of CS3 and a first chain in signal and wherein GCS2 is coupled to the PU(N) as a first PU input signal PUI(N).

35. (currently amended) The bi-directional bus of claim [[12]] 34, wherein CS4 is generated as a logic AND combination of GCS2 and a logic state of the chain out signal and GCS1 is generated as a logic AND combination of CS3 and a logic state of the chain in signal.

36. (currently amended) The bi-directional bus of claim [[12]] 34 wherein CS2 is generated as a logic OR combination of GCS1 and PUO(N) and GCS2 is generated as a logic OR combination of CS2 and CS1.

37. (currently amended) The bi-directional bus of claim [[6]] 36, wherein GCS2 is coupled as an input signal to PU(N).

38. (currently amended) The bi-directional bus of claim [[6]] 36, wherein the M PUs are pattern detection processing units, each for comparing input data to selected pattern data from pattern data stored in each of the M PUs and generating a compare output in each of the M PUs, wherein the selected pattern data in each of the M PUs is selected by an address pointer that is modified in response to a logic state of the compare output and an operation code stored with the selected pattern data.